CHARGE PUMP TYPE DC/DC CONVERTER

FIELD OF THE INVENTION

[0001] The present invention pertains to a charge pump type DC/DC converter.

BACKGROUND OF THE INVENTION

[0002] Typically, a DC/DC converter is used to convert a power supply voltage with an unstable level output from a DC power supply to a voltage with desired stable level. Since a charge pump type DC/DC converter uses capacitors as an energy storing element and needs no coil or reactor, it is small and inexpensive and has little EMI (electromagnetic interference). On the other hand, the voltage ripple is large, which is considered a problem.

[0003] FIG. 13 shows the theory of a conventional charge pump type DC/DC converter. This DC/DC converter is used for 1.5 times boosting. It has a voltage input terminal 122 connected to the output (positive) terminal of DC power supply 120, two flying capacitors C_a, C_b, capacitor C_s for smoothing, and voltage output terminal 124 connected to a load (not shown in the figure). Smoothing capacitor C_s is constantly connected between voltage output terminal 124 and the ground potential. Flying capacitors C_a, C_b switch alternately between the connection state of phase I shown in FIG. 13(A) and the connection state of phase II shown in FIG. 13(B).

[0004] More specifically, in phase I, two flying capacitors C_a, C_b are connected in series between voltage input terminal 122 and the ground potential in such a way that their positive terminals (+) face the side of voltage input terminal 122. In that connection state, two flying capacitors C_a, Cb are charged by the current flowing from DC power supply 120 to ground. In this case, when the capacitances of two flying capacitors C_a, C_b are set equal to each other, two flying capacitors C_a, C_b are charged to 0.5 V_{in} with respect to the output voltage of DC power supply 120, that is, the power supply voltage V_{in}. During that period, smoothing capacitor C_s is discharged to the load side via voltage output terminal 124 to maintain the supply of output voltage V_{out} to the load.

[0005] In phase II, two flying capacitors C_a, C_b are connected in parallel with each other between voltage input terminal 122 and voltage output terminal 124 in such a way that their positive

terminals (+) face voltage output terminal 124. In that connection state, a voltage of 1.5 V_{in} obtained by adding the charged voltage 0.5 V_{in} of two flying capacitors C_a, C_b to the power supply voltage V_{in} obtained from DC power supply 120 is supplied to the load and smoothing capacitor C_s via voltage output terminal 124.

[0006] In this DC/DC converter, when phases I and II are repeated and switched alternately, as shown in FIG. 14, an output voltage V_{out}, which approximately has a saw tooth waveform and decreases approximately monotonically in the period of phase I and increases approximately monotonically in the period of phase II, is obtained.

[0007] FIG. 15 shows the detailed circuit configuration of a DC/DC converter. In the switch circuit network shown in the figure, N-channel MOS transistors (referred to as "NMOS transistor" hereinafter) 126, 128, and 130 receive control signal ϕ from a switching control circuit (not shown in the figure) at their gate terminals and are turned on during the period of phase I and turned off during the period of phase II. On the other hand, NMOS transistors 132, 134, 136, and 138 receive control signal ϕ-, which has a phase difference of 180° from the control signal ϕ, from the switching control circuit at their gate terminals and are turned off during the period of phase I and turned on during the period of phase II.

[0008] As described above, in a conventional charge pump type DC/DC converter, although two flying capacitors C_a, C_b are connected to the current path from DC power supply 120 during the period of phase I, no current path is formed between DC power supply 120 and voltage output terminal 124. The output $voltage_{out}$, which is only dependent on the discharge of smoothing capacitor C_s, decreases at a relatively steep slope. As a result, a large voltage ripple occurs in the output $voltage_{out}$.

[0009] An general object of the present invention is to solve the problem of the conventional technology by providing a charge pump type DC/DC converter with an improved ripple characteristic in the output voltage.

SUMMARY OF THE INVENTION

[0010] This and other objects and features is provided, in accordance with one aspect of the invention by a charge pump type DC/DC converter having the following: a voltage input terminal connected to the output terminal of a DC power supply; first and second capacitors; a

voltage output terminal connected to a load; a switch circuit network having a first phase, in which a first terminal of the first capacitor is connected to the voltage input terminal, a first terminal of the second capacitor is connected to the voltage output terminal, and a second terminal of the first capacitor and a second terminal of the second capacitor are connected to each other, and a second phase, in which the first and second terminals of the first capacitor are connected to the voltage output terminal and the voltage input terminal, respectively, and the first and second terminals of the second capacitor are connected to the voltage input terminal and a reference potential, respectively; and a switching control means that controls the switch circuit network to switch the first and second phases alternately at prescribed duty ratios. The capacitors include a configuration having multiple capacitor elements.

[0011] In an aspect of the charge pump type DC/DC converter of the present invention, in the first phase, a current path is formed via the first and second capacitors between the voltage input terminal and the voltage output terminal. In the meantime when the first capacitor is charged by the current from the DC power supply, the second capacitor discharges to supply a load current to the side of the voltage output terminal. In the second phase, a current path is formed via the first capacitor between the voltage input terminal and the voltage output terminal, and a current path is formed via the second capacitor between the voltage input terminal and the reference potential (for example, the ground potential). The first capacitor discharges to supply a load current to the side of the voltage output terminal. On the other hand, the second capacitor is charged by the current from the DC power supply. Since a current path is formed between the voltage input terminal and voltage output terminal 14 and power is continuously supplied from the DC power supply to the load during both the first and second phases, the output voltage level can be maintained stably near the set voltage level.

[0012] According to another aspect of the present invention, the first capacitor is one capacitor element. In this case, it is preferred to set the capacitance of the first capacitor approximately equal to the capacitance of the second capacitor. Also, it is preferred to set the duty ratios of the first and second phases at about ½.

[0013] According to a further aspect of the present invention, the switch circuit network has a first MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the first capacitor, a second MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the first capacitor, a third MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the second

capacitor, a fourth MOS transistor with a first terminal connected to the second terminal of the first capacitor and a second terminal connected to the second terminal of the second capacitor, a fifth MOS transistor with a first terminal connected to the second terminal of the second capacitor and a second terminal connected to the reference potential, a sixth MOS transistor with a first terminal connected to the first terminal of the first capacitor and a second terminal connected to the voltage output terminal, and a seventh MOS transistor with a first terminal connected to the first terminal of the second capacitor and a second terminal connected to the voltage output terminal. In this case, the switching control means turns on the first, fourth, and seventh MOS transistors and turns off the second, third, fifth, and sixth MOS transistors in the first phase and turns off the first, fourth, and seventh MOS transistors and turns on the second, third, fifth, and sixth MOS transistors in the second phase.

[0014] According to yet another aspect of the present invention, the first capacitor is comprised of n (n is an integer of 2 or larger) capacitor elements. The n capacitor elements are connected in series in the first phase. In the second phase, the n capacitor elements are connected in parallel with each other. In this case, it is preferred that the n capacitor elements have approximately the same capacitance. It is also preferred to set the duty ratio of the first phase at about $1/(n+1)$ and to set the duty ratio of the second phase at about $n/(n+1)$. The boosting rate is defined as $\{1+1/(n+1)\}$. The boosting rate can be adjusted in a stepwise manner by changing the value of n.

[0015] According to a still further aspect of the present invention, when n=2, the first capacitor is comprised of first and second capacitor elements. The switch circuit network has a first MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the first capacitor element, a second MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the first capacitor element, a third MOS transistor with a first terminal connected to the second terminal of the first capacitor element and a second terminal connected to the first terminal of the second capacitor element, a fourth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the second capacitor element, a fifth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the second capacitor, a sixth MOS transistor with a first terminal connected to the second terminal of the second capacitor element and a second terminal connected to the second terminal of the second capacitor, a seventh MOS transistor with a first terminal connected to the second terminal of the second capacitor and a second terminal connected to the reference potential, an eighth MOS transistor with a first terminal connected to the first terminal of the first capacitor element and a

second terminal connected to the voltage output terminal, a ninth MOS with a first terminal connected to the first terminal of the second capacitor element and a second terminal connected to the voltage output terminal, and a tenth MOS transistor with a first terminal connected to the first terminal of the second capacitor and a second terminal connected to the voltage output terminal. In this case, preferably, the switching control means turns on the first, the third, the sixth, and the tenth MOS transistors and turns off the second, the fourth, the fifth, the seventh, the eighth, and the ninth MOS transistors in the first phase and turns off the first, the third, the sixth, and the tenth MOS transistors and turns on the second, the fourth, the fifth, the seventh, the eighth, and the ninth MOS transistors in the second phase.

[0016] According to a further aspect of the present invention, the first capacitor is comprised of n (n is an integer of 2 or larger) capacitor elements. The n capacitor elements are connected in parallel with each other in the first phase. In the second phase, the n capacitor elements are connected in series. In this case, it is preferred that the n capacitor elements have approximately the same capacitance. It is also preferred to set the duty ratio of the first phase at about n/(n+1) and to set the duty ratio of the second phase at about 1/(n+1). The boosting rate is defined as {2-1/(n+1)}. The boosting rate can be adjusted in a stepwise manner by changing the value of n.

[0017] According to another aspect of the present invention, when n=2, the first capacitor is comprised of first and second capacitor elements. The switch circuit network has a first MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the first capacitor element, a second MOS transistor with a first terminal connected to the second terminal of the first MOS transistor and a second terminal connected to the first terminal of the second capacitor element, a third MOS transistor with a first terminal connected to the second terminal of the first capacitor element and a second terminal connected to the first terminal of the second capacitor element, a fourth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the second capacitor element, a fifth MOS transistor with a first terminal connected to the second terminal of the first capacitor element and a second terminal connected to the second terminal of the second capacitor element, a sixth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the second capacitor, a seventh MOS transistor with a first terminal connected to the second terminal of the second capacitor element and a second terminal connected to the second terminal of the second capacitor, an eighth MOS transistor with a first terminal connected to the second terminal of the second capacitor and a second terminal connected to the reference potential, a ninth MOS transistor with a first terminal connected to the first terminal of the first

capacitor element and a second terminal connected to the voltage output terminal, and a tenth MOS transistor with a first terminal connected to the first terminal of the second capacitor and a second terminal connected to the voltage output terminal. In this case, the switching control means turns on the first, the second, the fifth, the seventh, and the tenth MOS transistors and turns off the third, the fourth, the sixth, the eighth, and the ninth MOS transistors in the first phase and turns off the first, the second, the fifth, the seventh, and the tenth MOS transistors and turns on the third, the fourth, the sixth, the eighth, and the ninth MOS transistors in the second phase.

[0018] According to a still further aspect of the present invention, the first capacitor is comprised of n x m (n and m are integers of 2 or larger) capacitor elements. In the first phase, for the n x m capacitor elements, all n capacitor elements are connected in series, and these serial capacitor circuits are connected in parallel in m columns. In the second phase, for the n x m capacitor elements, all m capacitor elements are connected in series, and these serial capacitor circuits are connected in parallel in n columns. In this case, it is preferred that the n x m capacitor elements have approximately the same capacitance. Also, it is preferred to set the duty ratio of the first phase at about m/(n+m) and to set the duty ratio of the second phase to about n/(n+m). The boosting rate is defined as {1+m/(n+m)} and can be adjusted in a stepwise manner by changing the values of n, m.

[0019] According to yet another aspect of the present invention, when n=2, m=2, the first capacitor is comprised of first, second, third, and fourth capacitor elements. The switch circuit network has a first MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the third capacitor element, a second MOS transistor with a first terminal connected to the first terminal of the third capacitor element and a second terminal connected to the first terminal of the first capacitor element, a third MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the first capacitor element, a fourth MOS transistor with a first terminal connected to the second terminal of the first capacitor element and a second terminal connected to the first terminal of the second capacitor element, a fifth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the second terminal of the second capacitor element, a sixth MOS transistor with a first terminal connected to the second terminal of the third capacitor element and a second terminal connected to the first terminal of the fourth capacitor element, a seventh MOS transistor with a first terminal connected to the first terminal of the first capacitor element and a second terminal connected to the second terminal of the third capacitor element, an eighth MOS transistor with a

first terminal connected to the first terminal of the second capacitor element and a second terminal connected to the second terminal of the fourth capacitor element, a ninth MOS transistor with a first terminal connected to the second terminal of the second capacitor element and a second terminal connected to the second terminal of the fourth capacitor element, a tenth MOS transistor with a first terminal connected to the voltage input terminal and a second terminal connected to the first terminal of the second capacitor, an eleventh MOS transistor with a first terminal connected to the second terminal of the fourth capacitor element and a second terminal connected to the second terminal of the second capacitor, a twelfth MOS transistor with a first terminal connected to the second terminal of the second capacitor and a second terminal connected to the reference potential, a thirteenth MOS transistor with a first terminal connected to the first terminal of the third capacitor element and a second terminal connected to the voltage output terminal, a fourteenth MOS transistor with a first terminal connected to the first terminal of the fourth capacitor element and a second terminal connected to the voltage output terminal, and a fifteenth MOS transistor with a first terminal connected to the first terminal of the second capacitor and a second terminal connected to the voltage output terminal. In this case, the switching control means turns on the first, the second, the fourth, the sixth, the ninth, the eleventh, and the fifteenth MOS transistors and turns off the third, the fifth, the seventh, the eighth, the tenth, the twelfth, the thirteenth, and the fourteenth MOS transistors in the first phase and turns off the first, the second, the fourth, the sixth, the ninth, the eleventh, and the fifteenth MOS transistors and turns on the third, the fifth, the seventh, the eighth, the tenth, the twelfth, the thirteenth, and the fourteenth MOS transistors in the second phase.

[0020] According to a further aspect of the present invention, in order to further reduce the ripple in the output voltage, a third capacitor for smoothing with a first terminal connected to the voltage output terminal and a second terminal connected to the reference potential is adopted. In addition, according to another preferable embodiment of the present invention, in order to further reduce the ripple in the output voltage and to finely set and adjust the output voltage, a current control circuit that is connected in series between the voltage input terminal and the first capacitor, a voltage detecting means used for detecting the output voltage obtained at the voltage output terminal, a reference voltage generating means that can generate a reference voltage corresponding to the set value of the output voltage output from the voltage output terminal, and a current control means that compares the output voltage detected by the voltage detecting means with the reference voltage and controls the current of the current control circuit corresponding to the comparison error are adopted. Also, it is preferred to turn off all the MOS transistors simultaneously in the phase switching period between the first and second phases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] FIG. 1 is a circuit diagram illustrating the theory of the charge pump type DC/DC converter disclosed in the first embodiment of the present invention.

FIG. 2 is a voltage waveform diagram schematically illustrating the waveform of the output voltage obtained in the first embodiment.

FIG. 3 is a circuit diagram illustrating an example of the switch circuit network used in the first embodiment.

FIG. 4 is a voltage waveform diagram comparing the simulated output voltage obtained in the first embodiment with the conventional example.

FIG. 5 is a circuit diagram illustrating the theory of the charge pump type DC/DC converter disclosed in the second embodiment of the present invention.

FIG. 6 is a voltage waveform diagram comparing the simulated output voltage obtained in the second embodiment with the conventional example.

FIG. 7 is a circuit diagram illustrating the theory of the charge pump type DC/DC converter disclosed in the third embodiment of the present invention.

FIG. 8 is a circuit diagram illustrating an example of the switch circuit network used in the third embodiment.

FIG. 9 is a circuit diagram illustrating the theory of the charge pump type DC/DC converter disclosed in the fourth embodiment of the present invention.

FIG. 10 is a circuit diagram illustrating an example of the switch circuit network used in the fourth embodiment.

FIG. 11 is a circuit diagram illustrating the theory of the charge pump type DC/DC converter disclosed in the fifth embodiment of the present invention.

FIG. 12 is a circuit diagram illustrating an example of the switch circuit network used in the fifth embodiment.

FIG. 13 is a circuit diagram illustrating the theory of a conventional charge pump type DC/DC converter.

FIG. 14 is a voltage waveform diagram schematically illustrating the waveform of the output voltage obtained by the conventional charge pump type DC/DC converter.

FIG. 15 is a circuit diagram illustrating the configuration of the switch circuit network used in the conventional charge pump type DC/DC converter.

REFERENCE NUMERALS AND SYMBOLS AS SHOWN IN THE DRAWINGS

[0022] In the figures, 10 represents a DC power supply, 12 a voltage input terminal, 14 a voltage output terminal, C_a, C_b flying capacitors, 16-28 NMOS transistors, 30 clock circuit, 32 a feedback circuit, 34 a current control circuit, 36 a resistance type voltage dividing circuit, 38 a reference voltage generating circuit, 40 a comparator, C_{a1}-C_{an} flying capacitor elements, 42-80 a NMOS transistors; C_{a11}... C_{an1}, C_{a1m}... C_{anm} flying capacitor elements, and 82-110 NMOS transistors

DESCRIPTION OF THE EMBODIMENTS

[0023] In the following, preferable embodiments of the present invention will be explained with reference to FIGS. 1-12.

[0024] FIG. 1 shows the theory of the charge pump type DC/DC converter disclosed in the first embodiment of the present invention.

[0025] This DC/DC converter is used for 1.5-times boosting. It has voltage input terminal 12 connected to the output (positive) terminal of DC power supply 10, a pair of flying capacitors C_a, C_b, each of which is constituted with one capacitor element, capacitor C_s for smoothing, and voltage output terminal 14 connected to a load (not shown in the figure). Smoothing capacitor C_s is constantly connected between voltage output terminal 14 and the ground potential. Flying

capacitors C_a, C_b are switched alternately between the connection state of phase I shown in FIG. 1(A) and the connection state of phase II shown in FIG. 1(B).

[0026] More specifically, in phase I, two flying capacitors C_a, C_b are connected in series between voltage input terminal 12 and voltage output terminal 14. In this case, the positive terminal of flying capacitor C_a is connected to voltage input terminal 12. The positive terminal of flying capacitor C_b is connected to voltage output terminal 14. The negative terminals (-) of the two flying capacitors C_a, C_b are connected to each other. In this connection state, flying capacitor C_a is charged by the current supplied from DC power supply 10, while flying capacitor C_b discharges to the side of the load. Smoothing capacitor C_s absorbs (charges) current from flying capacitor C_b or self-discharges to the load side corresponding to the voltage difference between the charged voltage and the output voltage of flying capacitor C_b and the voltage on the load side to reduce variation of output voltage V_{out}.

[0027] In phase II, flying capacitor C_a is connected between voltage input terminal 12 and voltage output terminal 14, while flying capacitor C_b is connected between voltage input terminal 12 and the ground potential. In this case, the positive terminal (+) of flying capacitor C_a is connected to voltage output terminal 14, while its negative terminal (-) is connected to voltage input terminal 12. The positive terminal (+) of flying capacitor C_b is connected to voltage input terminal 12, and its negative terminal (-) is connected to the ground potential. In this connection state, flying capacitor C_a discharges to the load side, while flying capacitor C_b is charged by current supplied from DC power supply 10. Smoothing capacitor C_s absorbs (charges) current from flying capacitor C_a or self-discharges to the load side corresponding to the voltage difference between its charged voltage and the output terminal of flying capacitor C_a and the voltage on the load side to suppress variation in output voltage V_{out}.

[0028] The output voltage V_{out} obtained at output voltage terminal 14 is derived as follows. When the charged voltages or voltage drops of flying capacitors C_a, C_b are represented by V_{Ca}, V_{Cb}, respectively, in phase II, equation (1) listed below becomes valid for flying capacitor C_a, while equation (2) listed below becomes valid for flying capacitor C_b.

$$V_{Ca} = V_{out} - V_{in} \ldots (1)$$

$$V_{Cb} = V_{in} \ldots (2)$$

[0029] In phase I, since flying capacitors C_a, C_b are connected in series between voltage input terminal 12 and voltage output terminal 14 as described above, equation (3) listed below becomes valid.

$$V_{out} = V_{in} - V_{ca} + V_{Cb} \ldots (3)$$

[0030] Equation (4) is obtained by substituting equations (1) and (2) into equation (3).

$$V_{out} = 1.5\ V_{in} \ldots (4)$$

[0031] In this embodiment, about 1.5-times boosting can be realized even if no special condition (C_a=C_b) is set for the capacitances of flying capacitors C_a, C_b.

[0032] When phases I and II are repeated and switched alternately in this DC/DC converter, as shown in FIG. 2, an output voltage$_{out}$ with approximately flat waveform having a stabilized voltage level in both periods of phases I and II is obtained. In other words, since a current path is formed between voltage input terminal 12 and voltage output terminal 14 in both phases I and II to supply current to the load without interrupting the power from DC power supply 10, the voltage level of output voltage V_{out} can be stably retained near the set value (about 1.5 V_{in}).

[0033] FIG. 3 shows an example of a switch circuit network used for realizing the switching between phases I and II in the embodiment described above. This switch circuit network includes two NMOS transistors 22 and 24 and 5 P-channel MOS transistors (referred to as "PMOS transistor" hereinafter) 16, 18, 20, 26, 28 as switching elements.

[0034] The source terminal of PMOS transistor 16 is connected to voltage input terminal 12, and its drain terminal is connected to the positive terminal of flying capacitor C_a. The source terminal of PMOS transistor 18 is connected to voltage input terminal 12, and its drain terminal is connected to the negative terminal of flying capacitor C_a. The source terminal of PMOS transistor 20 is connected to voltage input terminal 12, and its drain terminal is connected to the positive terminal of flying capacitor C_b. The drain terminal of NMOS transistor 22 is connected to the negative terminal of flying capacitor C_a, and its source terminal is connected to the negative terminal of flying capacitor C_b. The drain terminal of NMOS transistor 24 is connected to the negative terminal of flying capacitor C_b, and its source terminal is connected to the ground potential. The drain terminal of PMOS transistor 26 is connected to the positive terminal of flying capacitor C_a, and its source terminal is connected to voltage output terminal 14. The drain

terminal of PMOS transistor 28 is connected to the positive terminal of flying capacitor C_b, and its source terminal is connected to voltage output terminal 14.

[0035] A clock signal ϕ_N is sent from clock circuit 30 to the gate terminal of NMOS transistor 22. A clock signal ϕ_{N-} is sent from clock circuit 30 to the gate terminal of NMOS transistor 24. A clock signal ϕ_P is sent from clock circuit 30 to the gate terminals of PMOS transistors 16, 28. A clock signal ϕ_{P-} is sent from clock circuit 30 to the gate terminals of NMOS transistors 18, 20, and 26. The signal waveforms of clock signals ϕ_N, ϕ_{N-}, ϕ_P, ϕ_{P-} are shown in FIG. 3. ϕ_N is the reversed signal of ϕ_P. ϕ_{N-} is the reversed signal of ϕ_P-.

[0036] When PMOS transistor 26 is turned on, [the voltage at] the positive terminal of capacitor C_a becomes approximately equal to the output voltage. At that time, in order to prevent a short circuit between voltage output terminal 14 and voltage input terminal 12 as a result of turning on the parasitic diode of PMOS transistor 16, the back gate of PMOS transistor 16 is connected to the positive terminal of capacitor C_a. When PMOS transistor 26 is turned on, PMOS transistor 16 becomes inversely biased. When PMOS transistor 28 is turned on, the positive terminal of capacitor C_b becomes approximately equal to the output voltage. At that time, in order to prevent a short circuit between voltage output terminal 14 and voltage input terminal 12 as a result of turning on the parasitic diode of PMOS transistor 20, the back gate of PMOS transistor 20 is connected to the positive terminal of capacitor C_b. When PMOS transistor 28 is turned on, PMOS transistor 20 becomes inversely biased.

[0037] When ϕ_N, ϕ_{P-} are at H level and ϕ_{N-}, ϕ_P are at L level, transistors 16, 22, 28 are turned on, while transistors 18, 20, 24, and 26 are turned off. The connection state of phase I shown in FIG. 1(A) is obtained. If the period of the clock cycle (frequency F_{osc}) is taken as T_s ($1/F_{osc}$) and the H level duration time of ϕ_N (L level duration time of ϕ_P) is taken as T_ϕ, the duty ratio of phase I is defined as T_ϕ/T_s.

[0038] When ϕ_N, ϕ_P- are at L level and ϕ_{N-}, ϕ_P are at H level, transistors 16, 22, 28 are turned off, while transistors 18, 20, 24, and 26 are turned on. The connection state of phase II shown in FIG. 1(B) is obtained. If the H level duration time of ϕ_{N-} (L level duration time of ϕ_{P-}) is taken as $T_{\phi-}$, the duty ratio of phase II is defined as $T_{\phi-}/T_s$.

[0039] During the phase switching period from phase I to phase II or vice versa, it is preferred to set a period T_g, during which clock signals ϕ_N, ϕ_{N-} become L level simultaneously or clock signals ϕ_P, ϕ_{P-} become H level simultaneously, to turn off all of transistors 16-28 simultaneously.

[0040] By using the DC/DC converter disclosed in this embodiment, as described above, even if the capacitances of the two flying capacitors C_a, C_b are different, 1.5-times boosting can still be realized. However, the capacitances of the two flying capacitors or capacitor elements C_a, C_b are usually set at the same value. The duty ratios of the two phases I and II are also set equal to each other (about 0.5).

[0041] FIG. 4 compares the simulated output voltage waveform of the DC/DC converter disclosed in this embodiment with that of the conventional example (FIG. 15). V_{in}=2.4 V, C_a=C_b=0.1 μF, I_{out}=2 mA, F_{osc}= 100 kHz are set as the main conditions. The voltage ripple of the conventional example is about 12 mV. On the other hand, the voltage ripple of the embodiment is about 4 mV. The voltage ripple is reduced to about 1/3.

[0042] FIG. 5 shows the configuration of the main parts of the charge pump type DC/DC converter disclosed in the second embodiment. This embodiment adopts a feedback circuit 32 used for further stabilizing the voltage level of the output voltage V_{out} in the DC/DC converter disclosed in the first embodiment.

[0043] Said feedback circuit 32 has a current control circuit 34 connected between voltage input terminal 12 and flying capacitor C_a, a resistance type voltage dividing circuit 36 for voltage detection comprised of two resistors R1, R2 connected in series between voltage output terminal 14 and the ground potential, a reference voltage generator 38 that generates reference voltage V_{REF} corresponding to the set value of output voltage V_{out}, and a comparator 40 that compares the output voltage KV_{out} (K is a coefficient) of resistance type voltage dividing circuit 36 with reference voltage V_{REF} and outputs comparison error voltage ES.

[0044] Current control circuit 34 is, for example, constituted with a PMOS transistor. It controls the current supplied from DC power supply 10 to voltage output terminal 14 via flying capacitor C_a (or C_a, C_b) corresponding to the comparison error voltage ES sent from comparator 40 to its gate terminal. More specifically, when output voltage V_{out} is higher than the set level, the output (comparison error voltage) ES of comparator 40 is increased in proportion to the absolute value of the comparison error, and current control circuit 34 operates to reduce the current. When output voltage V_{out} is lower than the set level, the output (comparison error voltage) ES of comparator 40 is decreased in proportion to the absolute value of the comparison error, and current control circuit 34 operates to increase the current. Reference voltage generator 38 is, for example, constituted with a band gap circuit, which can adjust reference voltage V_{REF}.

[0045] FIG. 6(A) compares the simulated output voltage of the DC/DC converter disclosed in this embodiment (FIG. 5) with the conventional example (FIG. 15). FIG. 6(B) shows the output voltage waveform of the embodiment after the scale of the ordinate (output voltage) is enlarged. V_{in}=2.4 V, V_{out}=3.3 V, C_a=C_b=0.1 μF, I_{out}=2 mA, F_{osc}=100 kHz are set as the main conditions. The voltage ripple of the conventional example is about 11 mV. On the other hand, the voltage ripple of this embodiment is about 0.4 mV. The voltage ripple is reduced to about 1/28.

[0046] When said feedback circuit 32 is used, since the reference voltage V_{REF} of reference voltage generator 38 can be adjusted, it is possible to finely set or adjust the output voltage V_{out}.

[0047] As shown in FIG. 6(B), in this embodiment, the output voltage V_{out} drops instantaneously every half switching cycle. Said drop DR is caused for the following reason. During the period of switching from phase I to phase II or vice versa, all of transistors 16-28 in switch circuit network (FIG. 3) are turned off simultaneously. As a result, voltage output terminal 14 is cut off from the side of voltage input terminal 12 or DC power supply 10.

[0048] FIG. 7 shows the theory of the charge pump type DC/DC converter disclosed in the third embodiment of the present invention. In this embodiment, the first flying capacitor C_a is comprised of n (n is an integer of 2 or larger) capacitor elements C_{a1}, ..., C_{an}. In phase I, said n capacitor elements C_{a1}, ..., C_{an} are connected in series. In phase II, said n capacitor elements C_{a1}, ..., C_{an} are connected in parallel with each other. The remaining part is identical to the first or second embodiment.

[0049] More specifically, in phase I, as shown in FIG. 7(A), n capacitor elements C_{a1}, ... C_{an} are connected in series in such a way that the positive terminal of each capacitor element faces the side of voltage input terminal 12 to form one serial capacitor circuit. In phase II, as shown in FIG. 7(B), said n capacitor elements C_{a1}, ... C_{an} are connected in parallel with each other in such a way that the positive terminal of each capacitor element faces the side of voltage output terminal 14 to form one parallel capacitor circuit. It is preferred to set the capacitances of capacitor elements C_{a1}, ... C_{an} at the same value.

[0050] In this embodiment, the output voltage V_{out} obtained at voltage output terminal 14 is derived as follows. If the charged voltage or voltage drop of each of capacitor elements C_{a1}, ... C_{an} that constitute flying capacitor C_a is taken as V_{ca} and the charged voltage or voltage drop of

flying capacitor C_b is taken as V_{cb}, in phase I, equation (5) becomes valid for each capacitor element of flying capacitor C_a, and equation (6) becomes valid for flying capacitor C_b.

$$V_{ca} = V_{out} - V_{in} \ldots (5)$$

$$V_{cb} = V_{in} \ldots (6)$$

[0051] In phase I, when n flying capacitor elements $C_{a1}, \ldots, C_{an}$ and flying capacitor C_b are connected in series in the polarities between voltage input terminal 12 and voltage output terminal 14, equation (7) becomes valid.

$$V_{out} = V_{in} - nV_{ca} + V_{cb} \ldots (7)$$

[0052] Equation (8) can be derived as follows by substituting equations (5) and (6) into equation (7).

$$V_{out} = \{1+1/(n+1)\}V_{in} \ldots (8)$$

[0053] According to this embodiment, the boosting rate can be adjusted in a stepwise manner in a prescribed range of 1 (when $n=\infty$) – 1.33 (when n=2) corresponding to the number (n) of capacitor elements $C_{a1}, \ldots C_{an}$ that constitute the first flying capacitor C_a.

[0054] Since feedback circuit 32 is also adopted in this embodiment, the ripple in output voltage V_{out} can be further reduced, and the output voltage level can be finely set or adjusted.

[0055] The ratio of the load current supply ability between phase I, in which the n flying capacitor elements $C_{a1}, \ldots C_{an}$ of the first flying capacitor C_a are connected in series, and phase II, in which the capacitor elements are connected in parallel with each other, is 1:n. Consequently, by setting the duty ratios of phases I and II in a relationship (1:n) corresponding to the load current supply ability, that is, by setting the duty ratio of phase I to 1/(n+1) and setting the duty ratio of phase II to n/(n+1), the load current between the two phases I, II can be uniformized to minimize the voltage ripple.

[0056] FIG. 8 shows an example of the switch circuit network used in this embodiment when the first flying capacitor C_a is comprised of two capacitor elements C_{a1}, C_{a2} (n=2). This switch

circuit network includes 3 NMOS transistors 46, 52, 54 and 7 PMOS transistors 42, 44, 48, 50, 56, 58, 60 as switching elements.

[0057] The source terminal of PMOS transistor 42 is connected to voltage input terminal 12 via current control circuit 34, and its drain terminal is connected to the positive terminal of flying capacitor element C_{a1}. The source terminal of PMOS transistor 44 is connected to voltage input terminal 12 via current control circuit 34, and its drain terminal is connected to the negative terminal of flying capacitor element C_{a1}. The source terminal of NMOS transistor 46 is connected to the negative terminal of flying capacitor element C_{a1}, and its drain terminal is connected to the positive terminal of flying capacitor element C_{a2}. The source terminal of PMOS transistor 48 is connected to voltage input terminal 12 via current control circuit 34, and its drain terminal is connected to the negative terminal of flying capacitor element C_{a2}. The source terminal of PMOS transistor 50 is connected to voltage input terminal 12, and its drain terminal is connected to the positive terminal of flying capacitor C_b. The drain terminal of NMOS transistor 52 is connected to the negative terminal of flying capacitor element C_{a2}, and its source terminal is connected to the negative terminal of flying capacitor C_b. The drain terminal of NMOS transistor 54 is connected to the negative terminal of flying capacitor C_b, and its source terminal is connected to the ground potential. The drain terminal of PMOS transistor 56 is connected to the positive terminal of flying capacitor element C_{a1}, and its source terminal is connected to voltage output terminal 14. The drain terminal of PMOS transistor 58 is connected to the positive terminal of flying capacitor element C_{a2}, and its source terminal is connected to voltage output terminal 14. The drain terminal of PMOS transistor 60 is connected to the positive terminal of flying capacitor C_b, and its source terminal is connected to voltage output terminal 14.

[0058] Clock signal ϕ_N is sent from clock circuit 30 to the gate terminals of NMOS transistors 46, 52. Clock signal ϕ_{N-} is sent from clock circuit 30 to the gate terminal of NMOS transistor 54. Clock signal ϕ_P is sent from clock circuit 30 to the gate terminals of PMOS transistors 42, 60. Clock signal ϕ_{P-} is sent from clock circuit 30 to PMOS transistors 44, 48, 50, 56, 58. Clock signals ϕ_N, ϕ_{N-}, ϕ_P, ϕ_{P-} are identical to the clock signals shown in FIG. 3. For the same reason described for PMOS transistors 16 and 20 shown in FIG. 3, the back gates of PMOS transistors 42 and 50 are connected to the positive terminals of capacitor C_{a1} and capacitor C_b, respectively.

[0059] When ϕ_N, ϕ_{P-} are at H level and ϕ_{N-}, ϕ_P are at L level, transistors 42, 46, 52, and 60 are turned on, while transistors 44, 48, 50, 54, 56, and 58 are turned off. The connection state of phase I shown in FIG. 7(A) is obtained.

[0060] When ϕ_N, ϕ_{P-} are at L level and ϕ_{N-}, ϕ_P are at H level, transistors 42, 46, and 52 are turned off, while transistors 44, 48, 50, 54, 56, and 58 are turned on. The connection state of phase II shown in FIG. 7(B) is obtained.

[0061] In this embodiment, it is also possible to set a period, during which clock signals ϕ_N, ϕ_{N-} become L level simultaneously or clock signals ϕ_P, ϕ_{P-} become H level simultaneously, to turn off all of transistors 42-58 simultaneously.

[0062] FIG. 9 shows the theory of the charge pump type DC/DC converter disclosed in the fourth embodiment of the present invention. In this embodiment, the first flying capacitor C_a is comprised of n (n is an integer of 2 or larger) capacitor elements C_{a1}, ... , C_{an}. In phase I, said capacitor elements C_{a1}, ..., C_{an} are connected in parallel with each other. In phase II, said capacitor elements C_{a1}, ..., C_{an} are connected in series. The remaining part is identical to the first or second embodiment.

[0063] More specifically, in phase I, as shown in FIG. 9(A), n capacitor elements C_{a1}, ... C_{an} are connected in parallel with each other in such a way that the positive terminal of each capacitor element faces the side of voltage input terminal 12 to form one parallel capacitor circuit. In phase II, as shown in FIG. 9(B), said n capacitor elements C_{a1}, ... C_{an} are connected in series in such a way that the positive terminal of each capacitor element faces the side of voltage output terminal 14 to form one serial capacitor circuit. It is preferred to set the capacitances of capacitor elements C_{a1}, ... C_{an} at the same value.

[0064] In this embodiment, the output voltage V_{out} obtained at voltage output terminal 14 is derived as follows. The charged voltage or voltage drop of each of capacitor elements C_{a1}, ... C_{an} that constitute flying capacitor C_a is taken as V_{ca}, and the charged voltage or voltage drop of flying capacitor C_b is taken as V_{cb}. In phase II, equation (9) becomes valid for each capacitor element of flying capacitor C_a, and equation (10) becomes valid for flying capacitor C_b.

$$V_{ca} = (V_{out} - V_{in})/n \ldots (9)$$

$$V_{cb} = V_{in} \ldots (10)$$

[0065] In phase I, when n flying capacitor elements C_{a1}, ..., C_{an} and flying capacitor C_b are connected in series in the polarities between voltage input terminal 12 and voltage output terminal 14, equation (11) becomes valid.

$$V_{out} = V_{in} - V_{ca} + V_{cb} \ldots (11)$$

[0066] Equation (12) can be derived as follows by substituting equations (9) and (10) into equation (11).

$$V_{out} = \{2\text{-}1/(n+1)\}V_{in} \ldots (12)$$

[0067] According to this embodiment, the boosting rate can be adjusted in a stepwise manner in a prescribed range of 1.67 (when n=2) – 2 (when n=∞) corresponding to the number (n) of capacitor elements C_{a1}, ... C_{an} that constitute the first flying capacitor C_a.

[0068] Since feedback circuit 32 is also adopted in this embodiment, the ripple in output voltage V_{out} can be further reduced, and the output voltage level can be finely set or adjusted.

[0069] The ratio of the load current supply ability between phase I, in which the n flying capacitor elements C_{a1}, ... C_{an} of the first flying capacitor C_a are connected in parallel with each other, and phase II, in which the capacitor elements are connected in series, is n:1. Consequently, by setting the duty ratios of phases I and II in a relationship (n:1) corresponding to the load current supply ability, that is, by setting the duty ratio of phase I to n/(n+1) and setting the duty ratio of phase II to 1/(n+1), the load current between the two phases I, II can be uniformized to minimize the voltage ripple.

[0070] FIG. 10 shows an example of the switch circuit network used in this embodiment when the first flying capacitor C_a is comprised of two capacitor elements C_{a1}, C_{a2} (n=2). This switch circuit network includes 3 NMOS transistors 70, 74, 76 and 7 PMOS transistors 62, 64, 66, 68, 72, 78, 80 as the switching elements.

[0071] The source terminal of PMOS transistor 62 is connected to voltage input terminal 12 via current control circuit 34, and its drain terminal is connected to the positive terminal of flying capacitor element C_{a1}. The source terminal of PMOS transistor 64 is connected to the positive terminal of flying capacitor element C_{a1}, and the drain terminal is connected to the positive terminal of flying capacitor element C_{a2}. The drain terminal of PMOS transistor 66 is connected

to the negative terminal of flying capacitor element C_{a1}, and its source terminal is connected to the positive terminal of flying capacitor element C_{a2}. The source terminal of PMOS transistor 68 is connected to voltage input terminal 12 via current control circuit 34, and its drain terminal is connected to the negative terminal of flying capacitor element C_{a2}. The source terminal of NMOS transistor 70 is connected to the negative terminal of flying capacitor element C_{a2}, and its drain terminal is connected to the negative terminal of flying capacitor element C_{a1}. The source terminal of PMOS transistor 72 is connected to voltage input terminal 12, and its drain terminal is connected to the positive terminal of flying capacitor C_b. The drain terminal of NMOS transistor 74 is connected to the negative terminal of flying capacitor element C_{a2}, and its source terminal is connected to the negative terminal of flying capacitor C_b. The drain terminal of NMOS transistor 76 is connected to the negative terminal of flying capacitor C_b, and its source terminal is connected to the ground potential. The drain terminal of PMOS transistor 78 is connected to the positive terminal of flying capacitor element C_{a1}, and its source terminal is connected to voltage output terminal 14. The drain terminal of PMOS transistor 80 is connected to the positive terminal of flying capacitor C_b, and its source terminal is connected to voltage output terminal 14.

[0072] Clock signal ϕ_N is sent from clock circuit 30 to the gate terminals of NMOS transistors 70, 74. Clock signal ϕ_{N-} is sent from clock circuit 30 to the gate terminal of NMOS transistor 76. Clock signal ϕ_P is sent from clock circuit 30 to the gate terminals of PMOS transistors 62, 64, 80. Clock signal ϕ_{P-} is sent from clock circuit 30 to PMOS transistors 66, 68, 72, 78. Clock signals ϕ_N, ϕ_{N-}, ϕ_P, ϕ_{P-} are identical to the clock signals shown in FIG. 3. For the same reason described for PMOS transistors 16 and 20 shown in FIG. 3, the back gates of PMOS transistors 62 and 72 are connected to the positive terminals of capacitor C_{a1} and capacitor C_b, respectively.

[0073] When ϕ_N, ϕ_{P-} are at H level and ϕ_{N-}, ϕ_P are at L level, transistors 62, 64, 70, 74, and 80 are turned on, while transistors 66, 68, 72, 76, and 78 are turned off. The connection state of phase I shown in FIG. 9(A) is obtained.

[0074] When ϕ_N, ϕ_{P-} are at L level and ϕ_{N-}, ϕ_P are at H level, transistors 62, 64, 70, 74, and 80 are turned off, while transistors 66, 68, 72, 76, and 78 are turned on. The connection state of phase II shown in FIG. 9(B) is obtained.

[0075] In this embodiment, it is also possible to set a period, during which clock signals ϕ_N, ϕ_{N-} become L level simultaneously or clock signals ϕ_P, ϕ_{P-} become H level simultaneously, to turn off all of transistors 62-78 simultaneously.

[0076] FIG. 11 shows the theory of the charge pump type DC/DC converter disclosed in the fifth embodiment of the present invention. In this embodiment, the first flying capacitor C_a is comprised of n x m (n, m are integers of 2 or larger) capacitor elements C_{a1}, ..., C_{an}. In phase I, among said capacitor elements C_{a1}, ..., C_{an}, all n capacitor elements are connected in series, and these serial capacitor circuits are connected in parallel in m columns. In phase II, among said capacitor elements C_{a1}, ... C_{an}, all m capacitor elements are connected in series, and these serial capacitor circuits are connected in parallel in n columns. The remaining part is identical to the first or second embodiment.

[0077] More specifically, in phase I, as shown in FIG. 11(A), the n x m capacitor elements (C_{a11}, ..., C_{an1}), ..., (C_{a1m}, ..., C_{anm}) in the first flying capacitor C_a form m serial capacitor circuits with n capacitor elements in each circuit. Said m serial capacitor circuits are connected in parallel with each other. In this case, the positive terminal of each of capacitor elements C_{a11}, ..., C_{anm} faces the side of voltage input terminal 12. In phase II, as shown in FIG. 11(B), the n x m capacitor elements (C_{a11}, ..., C_{a1m}), ..., (C_{an1}, ..., C_{anm}) in the first flying capacitor C_a form n serial capacitor circuits with m capacitor elements in each circuit. Said n serial capacitor circuits are connected in parallel with each other. In this case, the positive terminal of each of capacitor elements C_{a11}, ..., C_{anm} faces the side of voltage output terminal 14. It is preferred to set the capacitances of capacitor elements C_{a11}, ... C_{anm} at the same value.

[0078] In this embodiment, the output voltage V_{out} obtained at voltage output terminal 14 is derived as follows. The charged voltage or voltage drop of each of capacitor elements C_{a11}, ..., C_{anm} that constitute flying capacitor C_a is taken as V_{ca}, and the charged voltage or voltage drop of flying capacitor C_b is taken as V_{cb}. In phase II, when each column of m capacitor elements, for example, (C_{a11}, ..., C_{a1m}) is connected in series in the polarity between voltage input terminal 12 and voltage output terminal 14, equation (13) becomes valid for each flying capacitor element. Also, equation (14) becomes valid for flying capacitor C_b connected in the polarity between voltage input terminal 12 and the ground potential.

$V_{ca} = (V_{out}-V_{in})/m$ ... (13)

$V_{cb} = V_{in}$ ... (14)

[0079] In phase I, when the serial capacitor circuit comprised of n flying capacitor elements, for example, (C_{a11}, ... C_{an1}) and flying capacitor C_P are connected in series in the polarity between voltage input terminal 12 and voltage output terminal 14, equation (15) becomes valid.

$V_{out} = V_{in} - nV_{ca} + V_{cb}$ ... (15)

[0080] Equation (16) can be derived by substituting equations (13) and (14) into equation (15).
$V_{out} = \{1+m/(n+m)\}V_{in}$ ... (16)

[0081] According to this embodiment, the boosting rate can be adjusted in a stepwise manner in a prescribed range of 1 (when $n=\infty$) – 2 (when $m=\infty$) corresponding to the number (n x m) of capacitor elements C_{a1}, ..., C_{anm} that constitute the first flying capacitor C_a.

[0082] Since feedback circuit 32 is also adopted in this embodiment, the ripple in output voltage V_{out} can be further reduced, and the output voltage level can be finely set or adjusted.

[0083] The ratio of the load current supply ability between phase I, in which the n x m flying capacitor elements C_{a11}, ... C_{anm} of the first flying capacitor C_a are connected in m columns that are parallel to each other, and phase II, in which the capacitor elements are connected in n columns that are parallel to each other, is m:n. Consequently, by setting the duty ratios of phases I and II in a relationship (m:n) corresponding to the load current supply ability, that is, by setting the duty ratio of phase I at m/(n+m) and setting the duty ratio of phase II at n/(n+m), the load current between the two phases I, II can be uniformized to minimize the voltage ripple.

[0084] FIG. 12 shows an example of the switch circuit network used in this embodiment when the first flying capacitor C_a is comprised of four capacitor elements C_{a11}, C_{a12}, C_{a21}, C_{a22} (n=2, m=2). This switch circuit network includes 15 NMOS transistors 82, 84, 86, 88, 90, 92, 94, 96, 98, 100, 102, 104, 106, 108, and 110 as switching elements.

[0085] The drain terminal of NMOS transistor 82 is connected to voltage input terminal 12 via current control circuit 34, and its source terminal is connected to the positive terminal of flying capacitor element C_{a21}. The drain terminal of NMOS transistor 84 is connected to the positive terminal of flying capacitor element C_{a21}, and its source terminal is connected to the positive terminal of flying capacitor element C_{a11}. The drain terminal of NMOS transistor 86 is connected to voltage input terminal 12 via current control circuit 34, and its source terminal is connected to the negative terminal of flying capacitor element C_{a11}. The source terminal of NMOS transistor 88 is connected to the negative terminal of flying capacitor element C_{a11}, and its drain terminal is connected to the positive terminal of flying capacitor C_{a12}. The drain terminal of NMOS transistor 90 is connected to voltage input terminal 12 via current control circuit 34, and its

source terminal is connected to the negative terminal of flying capacitor element C_{a12}. The source terminal of NMOS transistor 92 is connected to the negative terminal of flying capacitor element C_{a21}, and its drain terminal is connected to the positive terminal of flying capacitor element C_{a22}. The drain terminal of NMOS transistor 94 is connected to the positive terminal of flying capacitor element C_{a11}, and its source terminal is connected to the negative terminal of flying capacitor element C_{a21}. The drain terminal of NMOS transistor 96 is connected to the positive terminal of flying capacitor element C_{a12}, and its source terminal is connected to the negative terminal of flying capacitor element C_{a22}. The source terminal of NMOS transistor 98 is connected to the negative terminal of flying capacitor element C_{a12}, and its drain terminal is connected to the negative terminal of flying capacitor element C_{a22}. The drain terminal of NMOS transistor 100 is connected to voltage input terminal 12, and its source terminal is connected to the positive terminal of flying capacitor C_b. The drain terminal of NMOS transistor 102 is connected to the negative terminal of flying capacitor element C_{a22}, and its source terminal is connected to the negative terminal of flying capacitor C_b. The drain terminal of NMOS transistor 104 is connected to the negative terminal of flying capacitor C_b, and its source terminal is connected to the ground potential. The source terminal of NMOS transistor 106 is connected to the positive terminal of flying capacitor element C_{a21}, and its drain terminal is connected to the voltage output terminal. The source terminal of NMOS transistor 108 is connected to the positive terminal of flying capacitor element C_{a22}, and its drain terminal is connected to the voltage output terminal. The source terminal of NMOS transistor 110 is connected to the positive terminal of flying capacitor C_b, and its drain terminal is connected to the voltage output terminal.

[0086] Clock signal ϕ is supplied from clock circuit 30 to the gate terminals of NMOS transistors 82, 84, 88, 92, 98, 102, and 110. Clock signal ϕ- is supplied from clock circuit 30 to the gate terminals of NMOS transistors 86, 90, 94, 96, 100, 104, 106, and 108. The phase difference between the two clock signals ϕ and ϕ- is 180°.

[0087] When ϕ is at H level and ϕ- is at L level, NMOS transistors 82, 84, 88, 92, 98, 102, and 110 are turned on, while NMOS transistors 86, 90, 94, 96, 100, 104, 106, and 108 are turned off. The connection state of phase I shown in FIG. 11(A) is obtained.

[0088] When ϕ is at L level and ϕ- is at H level, NMOS transistors 82, 84, 88, 92, 98, 102, and 110 are turned off, while NMOS transistors 86, 90, 94, 96, 100, 104, 106, and 108 are turned on. The connection state of phase II shown in FIG. 11(B) is obtained.

[0089] In this embodiment, it is also preferred to set a period, in which both clock signals ϕ and ϕ- go to L level simultaneously, in the phase switching period to turn off all of NMOS transistors 82-110 simultaneously.

[0090] In the third-fifth embodiments described above, flying capacitor C_b can be constituted with one or several capacitor elements. Similarly, the smoothing capacitor C_s can also be constituted with one or several capacitor elements.

[0091] In the embodiments shown in FIGS. 3, 8, and 10, PMOS transistors and NMOS transistors are used in proper combination as the switching elements. However, it is also possible to only use NMOS transistors as described in the embodiment shown in FIG. 12. It is also possible to use PMOS transistors or other switching elements. In the embodiment shown in FIG. 12, it is also possible to use PMOS transistors and NMOS transistors in proper combination as the switching elements or use other switching elements.

[0092] As explained above, by using the charge pump type DC/DC converter disclosed in the present invention, the ripple characteristic of the output voltage can be improved significantly, and stepwise or fine adjustment of the boosting rate can be conducted easily. Also, compared with conventional technology, the ripple characteristic of the output voltage can be improved significantly without increasing the number of flying capacitors used.